

R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns an apparatus comprising one or more logic circuits configured to provide logical operation. The logic circuits may comprise (i) programmable logic elements and (ii) non-programmable logic elements within a programmable logic device (PLD). The programmable logic elements may be (i) configurable between two or more different logical functions and (ii) connectable by a routable interconnect circuit.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims and new claim 22 can be found in the specification on, for example, page 4 line 1-4, page 7, line 19 through page 8, line 4, page 8, line 10 through page 9, line 10, page 12, line 11 through page 13, line 11 and page 15, line 13 through page 16, line 6. As such, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-13 and 15-21 under 35 U.S.C. §102(b) as being anticipated by Ikawa et al. '686 (hereinafter

Ikawa) has been obviated by appropriate amendment and should be withdrawn.

Ikawa discloses a semiconductor integrated circuit device (Title of Ikawa). Ikawa discloses non-programmable logic elements (blocks 12-1, 12-2 ... 12-N in FIG. 1) with switching elements (elements 26 in FIG. 1).

In contrast, claim 1 of the present invention concerns one or more logic circuits comprising (i) programmable logic elements and (ii) non-programmable logic elements within a programmable logic device (PLD). The programmable logic elements may be (i) configurable between two or more different logical functions and (ii) connectable by a routable interconnect circuit. Claim 15 (means) and claim 16 (method) provide similar limitations.

Ikawa fails to disclose or suggest programmable logic elements that are configurable between two or more different logical functions. In particular, Ikawa explicitly discloses that the functional elements each have a predetermined logic function (Column 9, lines 51-56 and Claim 1(b) of Ikawa). As such, Ikawa does not disclose or suggest programmable logic elements that are configurable between two or more different logical functions as presently claimed. While the Office Action points to elements 26a-26n of Ikawa (switching FETs) as being programmable, the elements 26a-26n of Ikawa form switching elements, similar to the routable

interconnect circuit of the present invention. Even assuming, *arguendo*, with which Applicant's representative does not necessarily agree, that the switching FETs 26a-26n of Ikawa comprise programmable logic elements that are configurable between two or more different logical functions, then Ikawa still fails to disclose a routable interconnect circuit. In particular, the elements 26a-26n of Ikawa cannot be both the claimed programmable elements and the claimed routable interconnect circuit. Ikawa fails to disclose or suggest one or more logic circuits comprising (i) programmable logic elements and (ii) non-programmable logic elements within a programmable logic device (PLD), wherein the programmable logic elements are (i) configurable between two or more different logical functions, and (ii) connectable by a routable interconnect circuit. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claims 2-13 and 17-21 depended either directly or indirectly from independent claims 1 or 16 which are now believed to be allowable. As such, the presently pending invention is fully patentable over the cited reference and the rejection should be withdrawn.

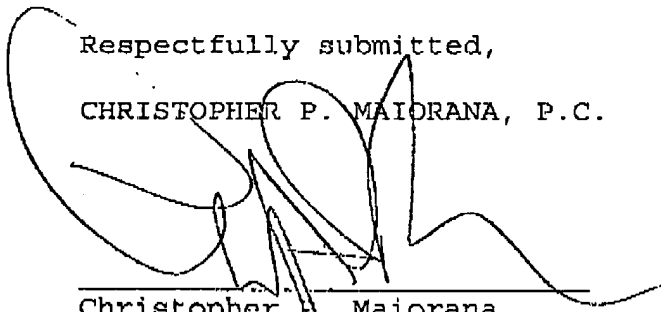
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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